

SM2258 B0KB F/W Release Note

| FW Package | MP Tool Version | ISP Version | Note |
|------------|--------------------|----------------|---|
| Q0518BS | Q0516A | Q0518BS | <ul style="list-style-type: none"> ● Add Kingston DRAM setting ● Add I/M FDh cmd to reset NAND when resuming from DevSLP ● Fix download ucode PIO mode can't return status issue ● Reload error retry count in each power cycle ● Fix SMART ID 0xF5 abnormal ● Disable all LUN pre-read function ● Change security state upon receiving Sanitize_Block_Erase_Ext CMD ● Add training ADJ ECC threshold |
| Q0308CS | Q0321B | Q0308CS | <ul style="list-style-type: none"> ● Support TCG function (enable by MP option). Industrial grade only. ● Add RDT retry pass count and maximum hard decode count to record RDT retry information. ● Info block add two pages RDT Retry Info and Hard Decode Info. ● Add SLC Whole Drive Scan condition, enable by MP option(CID offset 0x6F[6]). ● Fixed Progra Fail handle with SPOR case. |
| Q0125B | Q0125A | Q0125B | <ul style="list-style-type: none"> ● Fix drive hang issue when receiving STBY immediate without data in ● Modify Sanitize flow |
| Q0125A | Q0125A | Q0125A | <ul style="list-style-type: none"> ● Update power count when drive not in Device Sleep Resume or Download Microcode. ● Add Thermal Throttling function, enable by CID option offset 0x6F[7]. ● Modify HIPM/DIPM enable state. ● Fix Device Sleep when HIPM and DIPM not enabled. |
| Q0106A | Q0103A | Q0106A | <ul style="list-style-type: none"> ● Add Retry feature in NAND RDT. ● Add Vendor CMD to display DRAM/Flash/ASIC ODT and driving setting. ● Modify SATA error event log condition. |
| P1205A | P1202A | P1205A | <ul style="list-style-type: none"> ● Improve GC policy when dynamic SLC block exist. ● Improve pretest scenario regarding bad block0. ● Fix some multi-Lun NAND supporting issue. ● Optimize SATA phy setting |
| P1025A | P1025A | P1025A | <ul style="list-style-type: none"> ● Add "Enable Cache Program" option to enhance performance for 128GB Drive. ● Extend RDT error count from 256 to 1024 ● Fix some INTEL L06B to B0KB NAND issues ● Fix retry hang issue when fail large than 2 plane case. ● Save total SLC bad count when mark bad event occurs. ● Fix pure SLC block calculation. |
| P0925A | P1004A | P0925A | <ul style="list-style-type: none"> ● Add the ID check for the switch between Intel L06B and B0KB. ● Add CID option (offset 0x63[3]) to enable/disable Micron trim register (default enable). ● Enhance RDT read/write and check flow. ● Add RDT result information of total BB block count by CH/CE, TLC start block, and RDT threshold settings. ● Update MIRA DRAM timing settings. |
| P0824A | P0824A | P0824A | <ul style="list-style-type: none"> ● Update CID default settings ● Bug fix of 3 dies configuration issue ● Add more RDT result information |

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| | | | <ul style="list-style-type: none"> ● Add MIRA DRAM setting ● Enable prepare fast boot when sleep command |
| P0801B | P0729A | P0801B | <ul style="list-style-type: none"> ● Bug fixes of RDT failure and enhancement of RDT for NAND and DRAM self-test. ● Enable switchable NAND I/O DDR400/DDR200 by CID. ● Bug fix of SPOR and DEVSLP issues. |
| P0718A | P0715A | P0718A | <ul style="list-style-type: none"> ● Initial enablement of Intel B0KB. ● Fixes of SPOR issue. ● Enrich MP Tool features for efficient MFG. ● Enhance RDT function for MFG. |
| P0603 | P0531A | P0603 | <ul style="list-style-type: none"> ● Initial enablement of Micron B0KB. |

Note:

1. F/W and ISP update is recommended.
2. History # is denoted by "Version-Date".

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